

CONTINUOUS DEEP ANALYTICS (2018-2023)







> Lars Kroll

<u>Systems</u>

Machine

Learning



prog.languages distr. computing

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data stream proc.

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compilers prog. languages distr.computing constraint prog. distr. systems

New MSc/PhDs

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Tensor Programming

Relational Data Streams



Dynamic Graphs



Hardware Acceleration: Important but <u>Not Enough</u>

critical decision making

Pipeline (CPU)

Pipeline (GPU/TPU)





Cross-Platform Computation is Inefficient

- No computation sharing optimisations



- expensive data exchange through disk



Computation Sharing



+no additional overhead



Critical Decision Making demands **Efficiency**

critical decision making

Pipeline (CPU)	
Pipeline (CPU) - Optimised	
Pipeline (GPU/TPU)	
Pipeline (GPU/TPU) - Optimised	







The Problem



Python™

TensorFlow

f

f

Intermediate Representation **(IR)**

• • • • • • • • • • •

The Solution





IR







Model and Language Independence

Data Pipeline



A Distributed Runtime for Heterogeneous HW







Rust-Based







Target Architecture





Distributed JIT Compilation

Discovered better Plan

constraint solver (instruction selection)

Change in Resources

Change in Load Distribution

Monitoring









From Weld IR for Streaming

Lars Kroll - KTH









- A restrictive language for describing data transformations • Pure expressions without side effects
- A compiler that produces LLVM IR
- Compiler leverages Weld's declarative syntax to make optimisations

What is Weld? Data B



OF TECHNOLOGY

- Scalar+SIMD types
 - bool, u8...u64, i8...i64, f32, f64
- **Collections:** Read-only data types
 - vec, dict
- **Builders:** Write-only data types
 - appender, merger, groupbuilder
 - additive monads
- Structs { ... }: more like Tuples really
 - Builders are compositional over structs
 - I.e. structs of builders are also builders

Weld IR - Types

No read-write data types!



- result turns a builder into the corresponding type, i.e.
 - appender [i32] into vec [i32]
 - merger[i32,+] into i32 (sum)
 - In Weld you may only call result on a builder once and it consumes the builder (linear type)
- if, lookup, math functions, binary ops, casts, c-udfs, etc.

Weld IR - Ops

• for is a parallel loop over a collection (or iterator) and into a builder

• merge consumes a builder and a value and produces a new builder with the value merged in (according to the builder's semantics)



Weld Compilation

- Online (~JIT) compilation
- front-ends (e.g., Python)
- Monadic properties allow automatic parallelisation and vectorisation
- fusion and filter reordering

• Quick and easy type inference to support dynamically typed

• Declarative style allows data access optimisations, such as loop



OF TECHNOLOGY

Scala input.map(i: Int => i + 5)

Weld |input:vec[i32]|

result(for (input, appender[i32], lapp, , i| merge(app, i + 5))

Weld Example



Scala input.map(i: Int => i + 5)

Weld |input:vec[i32]| result(for(input:vec[i32], appender[i32], merge(app, i + 5))

Weld Example

|app:appender[i32], :i64, i:i32|





- Arc extends Weld for streaming
- Observation
 - Stream Sources are read-only
 - Stream Sinks are write-only
 - Connect Sinks to Sources via Channels
- Source is a collection stream [T]
- Sink is a builder streamappender [T]

Arc

• Calling result on a Sink returns a Source and creates a Channel between them



Arc Example I

Scala input.map(i: Int => i + 5)

Arc |source:stream[i32], sink: streamappender[i32]| for (source, sink, out, i merge(out, i + 5))



Arc Example 2 Scala input.filter(i: Int => i > 5)

Arc |source:stream[i32], sink: streamappender[i32]|
 for(source,
 sink,
 |out, i|
 if (i > 5, merge(out, i), out))





Scala val mapped = input.map(i: Int => i + 5)

Arc |source:stream[i32], evenSink:streamappender[i32], oddSink:streamappender[i32] let mapped = result(for(source, streamappender[i32], for (mapped, evenSink, |out, i| for (mapped, oddSink, |out, i|

Arc Example 3

- mapped.filter(i: Int => i % 2 == 0).toSink(...) mapped.filter(i: Int => i % 2 != 0).toSink(...)
 - |out, i| merge(out, i + 5));if (i % 2 == 0, merge(out, i), out)); if (i % 2 != 0, merge(out, i), out))



Arc Example 3

Scala val mapped = input.map(i: Int => i + 5)

Arc |source:stream[i32], evenSink:streamappender[i32], oddSink:streamappender[i32] for (source, {evenSink, oddSink}, out, i let j = i + 5;if (j & 2 == 0),

- mapped.filter(i: Int => i % 2 == 0).toSink(...) mapped.filter(i: Int => i % 2 != 0).toSink(...)

 - {merge(out.\$1, j),out.\$2}, {out.\$1, merge(out.\$2, j)})



Arc Windows

- Windows are supported using higher-order builders (windower)
- In addition to merge-type and result-type, a windower also has an aggregation-type, which must be another builder
- Use Weld functions to
 - determine window start and end points,
 - convert the aggregation-type into the result-type
 - convert the windower's merge-type into the aggregation-builder's merge-type



Arc Compilation

- Ahead-of-time compilation
- Target long-running jobs (allow costly optimisations)
- Constraint-based type-inference solver
- Compile to a deployment graph IR (and from there to Rust)
- Leave pure Weld expressions to the Weld compiler
- Declarative style allows data flow optimisations, such as operator fusion and filter reordering